REMARKS

Claims 1-10 are pending in this application and are rejected. In response, Applicants are amending claims 1-10 and add new claims 11-14. No new matter is introduced by the amended claims and newly added claims 11-14, which are fully supported by the specification. In view of the following remarks, Applicants respectfully request reconsideration of the application.

Claim Objection

In paragraph 1, the Examiner objected to claim 8 for a misspelling of "parallel." Applicants amend claim 8 and respectfully submit that the amended claim overcomes the objection. Therefore, Applicants respectfully request the withdrawal of the objection.

Rejection under 35 U.S.C. § 112

In paragraph 2, the Examiner rejected claims 7-10 under 35 U.S.C. § 112 for indefiniteness. Applicants amend claims 7-10 and respectfully submit that the amended claims particularly point out and distinctly claim the invention.

Specifically, in claim 7, the claimed limitation of "switchably connectable" is no longer recited. Therefore, Applicants respectfully request the withdrawal of the rejection and reconsideration of claims 7-10.

Rejections under 35 U.S.C. § 102(e)

In paragraph 3, claims 1-5 and 7-9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Mackre, U.S. Patent No. 6,128,317. Applicants respectfully traverse.

Regarding independent claim 1, the Examiner states that "Mackre discloses an apparatus for interconnecting a plurality of signal endpoints..." However, amended claim 1 recites "at least one barrel shift register" coupled to an endpoint. A barrel shift register has the ability to shift many bits at the same time and can provide multiple outputs. In contrast, a shift register, such as the one used in Mackre, can typically only shift one bit per cycle and typically provides only one output. Since Mackre does not disclose a "barrel shift register," Mackre cannot anticipate the Applicants' invention. Therefore, claim 1 is not anticipated by Mackre.

Regarding independent claim 7, on page 4, last paragraph, lines 4 and 5, the Examiner equates "signals provided to a plurality of barrel shift registers" to "signal[s] being received by shift registers." However, the method recited in claim 7 uses barrel shift registers, which may shift many bits at the same time and can also provide multiple outputs. Typically, shift registers shift one bit at a time and provide only one output. Therefore, Mackre cannot anticipate the method recited in claim 7 for providing signals to a plurality of barrel shift registers. Applicants respectfully request reconsideration of claim 7 since Mackre cannot anticipate claim 7.

Similarly, newly added independent claim 14 is allowable for the same reason as allowable claims 1 and 7. The means for providing signals to a plurality of barrel shift registers is different from the means for receiving signals by shift registers. Therefore, Mackre cannot anticipate the use of the barrel shift registers in claim 14.

Dependent claims 2-6 depend either directly or indirectly from claim 1. Similarly, dependent claims 8-10 depend directly from claim 7. Since independent claims 1 and 7 are allowable, the dependent claims are allowable for the same reason.

Rejections under 35 U.S.C. § 103(a)

In paragraph 4 of the Office Action, claims 6 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mackre. Applicants respectfully traverse. Amended independent claims 1 and 7, from which claims 6 and10 depend from, respectively, recite a "barrel shift register" which is not disclosed in Mackre. Further, Mackre discloses in FIG. 3 the use of "shift registers" with multiple gate levels. However, the use of multiple gates is undesirable in the present invention (see Background of the Invention and page 8, lines 10-16). Therefore, the use of shift registers in Mackre teaches away from the present invention. Because claims 6 and 10 depend from claims 1 and 7, which are not obvious in view of Mackre, claims 6 and 10 are also not obvious.

Conclusion

Based on the above remarks, the Applicants believe that they have fully overcome the objection and rejections in the Office Action of March 26, 2002 and that the application is in condition for allowance. If the Examiner has questions regarding the case, the Examiner is invited to contact the Applicants' undersigned representative at the number given below.

Respectfully submitted,

Seng-Khoon Tng et al.

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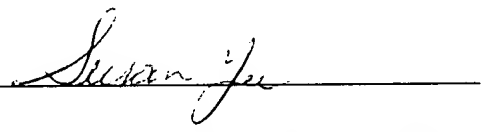
By: 

Susan Yee, Reg. No. 41,388
Carr & Ferrell, LLP
2225 E. Bayshore Road, Suite 200
Palo Alto, CA 94303
Tel: (650) 812-3423
Fax: (650) 812-3444

Version with markings to show changes made

In the Claims:

1. (Once amended) [Electrical] An electronic switching apparatus for flexibly interconnecting a plurality of signal endpoints, the apparatus comprising:

a first circuit for receiving at least one input signal from at least one input endpoint, the first circuit having at least one barrel shift register coupled to at least one of the at least one input endpoint for receiving the at least one input signal, shifting and rotating the at least one input signal, and transmitting at least one output signal; and

a second circuit coupled to outputs from the first circuit for sending at least one received signal to at least one output endpoint.

2. (Once amended) The electronic switching apparatus of [C]claim 1, wherein[:] the at least one input signal comprises a data signal that is received in serial form including a plurality of data channels interleaved therein.

3. (Once amended) The electronic switching apparatus of [C]claim 2, wherein[: the first circuit comprises at least one barrel shift register for receiving at least one received input signal which comprises serial data, and] the second circuit further comprises at least one multiplexer[,] selectably coupled to the at least one [such] barrel shift register [being selectably coupled to at least one such multiplexer,] thereby effectively enabling digital signal switching simultaneously between [multiple] the at least one input endpoint and the at least one output endpoint[s].

4. (Once amended) The electronic switching apparatus of [C]claim 1, wherein[:] the at least one input signal comprises a data signal that is received in parallel form and converted to serial form.

5. (Once amended) The electronic switching apparatus of [C]claim 2, wherein[: the first circuit comprises a] the barrel [shifter] shift register [for] interconnect[ing]s a plurality of received input signals at different times.

6. (Once amended) The electronic switching apparatus of [C]claim 1, wherein[:] the at least one [of the] input endpoint or the at least one output endpoint[s] corresponds to at least one pin for a coder/decoder (codec) device, such codec device being compliant with an AC97 or an I2S convention.

7. (Once amended) A [M]method for electronic signal coupling, the method comprising the steps of:

receiving a first set of digital signals, the received first set of digital signals being provided to a plurality of barrel shift registers;

shifting and rotating the first set of digital signals; and

transmitting a second set of digital signals, the transmitted second set of digital signals being provided from a plurality of multiplexers[;

wherein], the plurality of multiplexers [are switchably connectable] being selectably coupled to the barrel shift registers[,] such that at least one signal selected in the first set of digital signals is selectably [interconnected] coupled for transmission in the second set of digital signals.

8. (Once amended) The method of [C]claim 7, wherein[:] the first set of digital signals comprises a data signal which is received in either serial or parallel form, the data signal being converted to serial form when received in parallel form.

9. (Once amended) The method of [C]claim [8]7, wherein[:] a plurality of digital signals in the first set of digital signals are transmitted as digital signals in the second set of digital signals separately at different times.

10. (Once amended) The method of [C]claim [8]7, wherein[:] at least one transmitted digital signal from the second set of digital signals is coupled to at least one pin associated with a coder/decoder (codec) according to an AC97 or I2S signal interface.